AMENDMENT TO THE CLAIMS:

LISTING OF CLAIMS:

This listing of claims replaces all prior versions, and listings, of claims in the referenced application.

Claims 1-5 cancelled.

Claim 6. (Currently amended, Allowable)) A tri-stable CMOS latch, having first and second inputs for receiving first and second input signals, respectively, where the first and second input signals have first and second signal levels, and with combinations of the signal levels of the first and second input signals defining first, second, and third ternary logic states, said tri-stable CMOS latch ~~ternary logic signals in either a first, second, or third state~~, comprising:

a first series circuit coupling first and second supply voltage terminals, with the first series circuit including a first PMOS transistor, including source, drain, and gate terminals coupling the first supply voltage terminal to a first node, a first biasing element coupling the first node to a second node, and a first NMOS transistor, including source, drain, and gate terminals coupling the second node to the second supply voltage terminal;

a second series circuit coupling the first and second supply voltage terminals, with the second series circuit including a second PMOS transistor, including source, drain, and gate terminals coupling the first supply voltage terminal to a third node, a second biasing element coupling the third node to a fourth node, and a second NMOS transistor, including source, drain, and gate terminals coupling the fourth node to the second supply voltage terminal;

a feedback network coupling the first node to the gate terminal of the second NMOS transistor, the second node to the gate terminal of the second PMOS transistor, the third node to the gate terminal of the first NMOS transistor, and the fourth node to the gate terminal of the first PMOS transistor;

with said first and second biasing elements, and said MOS transistors fabricated utilizing MOSFET technology, where said first and second biasing elements are diode-connected transistors, and with the first and second biasing elements creating unequal

voltage drops to bias the PMOS and NMOS transistors in one of the first and second series circuits in a higher-current state and the PMOS and NMOS transistor of the other of the first and second series circuits in a lower-current state to achieve first and second stable operating points when the first and second input signals having signal levels defining a ternary signal in the first or second ternary logic states are ~~is~~ received and creating substantially identical voltage drops to bias the PMOS and NMOS transistors in both the first and second series circuits in triode mode to achieve a third stable operating point, where the first and second PMOS and NMOS transistors conduct substantially the same current, when the first and second input signals having signal levels defining ~~a ternary logic signal in~~ the third ternary logic state are ~~is~~ received.

Claim 7. (Thrice amended, Allowable) A MOS circuit comprising:

a current source;

a first clocking transistor having source, drain, and gate terminal with said source terminal coupled to the current source, where the first clocking transistor conducts when a first control signal, received at said gate terminal, is asserted;

a tristable MOS latch including:

first and second inputs for receiving first and second input signals, respectively, where the first and second input signals have first and second signal levels, and with combinations of the signal levels of the first and second input signals defining first, second, and third ternary logic states ~~ternary logic signals in either a first, second, or third state~~;

a first series circuit coupling a first supply voltage terminal to the drain terminal of said first clocking transistor, with the first series circuit including a first load element coupling the first supply voltage terminal to a first node, a first biasing element coupling the first node to a second node, and a first MOS transistor, including source, drain, and gate terminals coupling the second node to the drain terminal of said first clocking transistor;

a second series circuit coupling a first supply voltage terminal to the drain terminal of said first clocking transistor, with the second series circuit including a second load element coupling the first supply voltage terminal to a third node, a second biasing element coupling the third node to a fourth node, and a second MOS

transistor, including source, drain, and gate terminals coupling the fourth node to the drain terminal of said first clocking transistor;

a feedback network coupling the first node to the gate terminal of the second MOS transistor and third node to the gate terminal of the first MOS transistor;

with said first and second load elements, said biasing elements, and said MOS transistors fabricated utilizing MOSFET technology and with the first and second load and biasing elements creating unequal voltage drops to bias one of the MOS transistors in a higher-current state and the other MOS transistor in a lower-current state to achieve first and second stable operating points when the first and second input signals having signal levels defining ~~a ternary signal in~~ the first or second ternary logic states are ~~is~~ received and creating substantially identical voltage drops to bias the MOS transistors in triode mode to achieve a third stable operating point, where the first and second MOS transistors conduct substantially the same current, when the first and second input signals having signal levels defining ~~a ternary logic signal in~~ the third ternary logic state are is received;

a second clocking transistor having source, drain, and gate terminal with its source terminal coupled to the current source, where the second clocking transistor conducts when a second control signal, received at said gate terminal, is asserted;

an input circuit including:

first and second circuits respectively coupling the first and third nodes to the drain terminal of the second clocking transistor, with the first circuit including a first input transistor having source, drain, and gate terminals, the first input transistor coupled to the first input to receive a first input signal at said gate terminal and with the second circuit including a second input transistor having source, drain, and gate terminals, the second input transistor coupled to the second input to receive a second input signal at said gate terminal;

where the tristable latch holds any of the first, second, or third ternary logic states applied to the first and second inputs when the first control signal is a asserted and the second control signal is not asserted.

Claim 8 and 9. (Cancelled)